CLAIMS

What is claimed is:

1. A memory cell comprising:
   a chalcogenide random access memory (CRAM) cell; and
   a CMOS circuit operative to access the CRAM cell.

2. The memory cell of claim 1, wherein the CRAM cell has cross-sectional area determined by a thin film process and by an iso-etching process.

3. The memory cell of claim 2, wherein the CRAM cell has cross-sectional area determined by a chalcogenide deposition thin film process and by an iso-etching process.

4. The memory cell of claim 1, wherein the CRAM cell further comprises a chalcogenide structure in series with a semiconductor device.

5. The memory cell of claim 4, wherein the semiconductor device is a diode operative to drive a current through the chalcogenide structure.

6. The memory cell of claim 4, wherein the semiconductor device is a selecting transistor operative to drive a current through the chalcogenide structure when enabled by a voltage at a gate terminal of the selecting transistor.

7. The memory cell of claim 6, wherein:
   the gate terminal of the selecting transistor is operatively coupled to a word line of a memory array;
   a source terminal of the selecting transistor is operatively coupled to a drive line of the memory array; and
   the drain terminal of the selecting transistor is operatively coupled to a bit line of the memory array.

8. A memory array comprising:

a plurality of chalcogenide random access memory (CRAM) cells;

a plurality of word lines each of which is operative to assert a data word, comprising a subset of the CRAM cells, in response to a CMOS circuit; and

a plurality of bit lines each of which is operative to access a CRAM cell of the plurality of CRAM cells, in response to an assertion of a word line.

9. The memory array of claim 8, wherein each of the CRAM cells of the plurality of CRAM cells has a cross-sectional area determined by a thin film process and by an iso-etching process.

10. The memory array of claim 9, wherein each of the CRAM cells of the plurality of CRAM cells has a cross-sectional area determined by a chalcogenide deposition thin film process and by an iso-etching process.

11. The memory array of claim 8, wherein each of the CRAM cells of the plurality of CRAM cells further comprises a chalcogenide structure in series with a semiconductor device.

12. The memory array of claim 11, wherein the semiconductor device is a diode operative to drive a current through the chalcogenide structure.

13. The memory array of claim 11, wherein the semiconductor device is a selecting transistor operative to drive a current through the chalcogenide structure when enabled by a voltage at a gate terminal of the selecting transistor.

14. The memory array of claim 13, wherein:

the gate terminal of the selecting transistor is operatively coupled to a word line of a memory array;

a source terminal of the selecting transistor is operatively coupled to a drive line of the memory array; and

the drain terminal of the selecting transistor is operatively coupled to a bit line of the memory array.

15. A method for fabricating a memory cell comprising steps of:

depositing a chalcogenide structure on a substrate to form a chalcogenide random access memory (CRAM) cell;

using a thin film process, determining a height of the chalcogenide structure;

using an iso-etching process, determining a width of the chalcogenide structure, such that the chalcogenide structure has a cross-sectional area determined by the thin film process and by the iso-etching process; and

coupling the chalcogenide structure to a CMOS circuit operative to access the CRAM cell.

18. The method for fabricating a memory cell of claim 15, further comprising a step of depositing a semiconductor device in series with the CRAM cell.

19. The method for fabricating a memory cell of claim 18, wherein the step of depositing a semiconductor device includes a step of fabricating a diode operative to drive a current through the chalcogenide structure.

20. The method for fabricating a memory cell of claim 18, wherein the step of depositing a semiconductor device includes a step of fabricating a selecting transistor operative to drive a current through the chalcogenide structure when enabled by a voltage at a gate terminal of the selecting transistor.

21. The method for fabricating a memory cell of claim 18, wherein the step of depositing a semiconductor device includes steps of:

fabricating a gate terminal of the selecting transistor to be operatively coupled to a word line of a memory array;

fabricating a source terminal of the selecting transistor to be operatively coupled to a drive line of the memory array; and

fabricating the drain terminal of the selecting transistor to be operatively coupled to a bit line of the memory array.